REMARKS/ARGUMENTS

This is intended as a full and complete response to the Office Action dated September 25, 2003, having a shortened statutory period for response set to expire on December 25, 2003 (the "Office Action"). Claims 1-28 remain pending in the application.

At the outset, it is noted in the Office Action that changes made to 35 U.S.C. 102(e) by the American Inventors Protection Action of 1999 ("AIPA") do not apply. However, this application was filed after November 29, 2000, and thus it is believe that
35 U.S.C. 102(e) as amended by the AIPA is applicable.

In the Office Action, claims 1-28 were rejected under 35 U.S.C. 102(e) as being anticipated by Lien *et al.* (U.S. Pat. No. 6,301,696; "Lien"). Applicant respectfully disagrees with the rejection of claims 1-28 as being anticipated by Lien for the below set forth reasons. However, prior to reaching the rejections, reaching an understanding of what is disclosed by Lien is appropriate.

Lien discloses "hardening" an FPGA. (See generally, Lien at col. 4, lines 50-57.) The hardened FPGA may be embedded in a larger integrated circuit. (See generally, Lien at col. 5, lines 9-33, and at col. 6, lines 37-47.) In the hardening process, metal connections are used to bypass selected transistors during the manufacturing process of the FPGA. (See generally, Lien at col. 5, lines 33-47 and at col. 6, lines 27-36.) The "conservation of the underlying physical template of the FPGA with substantially no reduction in silicon area" is a suggested result in Lien. (Lien at col. 5, lines 58-59.) This point is stated and restated in Lien stating with reference to the FPGA that "the underlying physical template is not changed". (See generally, Lien at col. 7, lines 1-28.) Lien then goes on to disclose "two general ways to make the connection between source and drain terminals of a transistor during a

semiconductor manufacturing process." (See, Lien at col. 8, lines 1-18.) Lien then goes on to provide examples for forming metal lines to bypass a transistor or to create a dedicated connection to provide a selected signal for a selection circuit. (See generally, Lien at col. 8, lines 39-67 with reference to Figs. 8A-C, and at col. 9, lines 1-57 with reference to Figs. 9A-B.) In short, Lien discloses creating dedicated connections for a design instantiated in an FPGA, where the underlying circuit template of the FPGA is unchanged.

Thus, Lien is directed to modifying an FPGA, which may then be embedded in a larger integrated circuit, to provide an embedded hardened FPGA core. However, Lien is not about how to interconnect the embedded FPGA with the larger integrated circuit. Bypassing transistors with metal lines of an underlying device, particularly with respect to lines that are all on pitch to the underlying unchanged structure, is not what is being claimed in pending claims 1-28.

Now, turning attention to the rejection of the claims, in the Office Action it is stated in part that Lien discloses a method for configuring a routing program with respect to the rejection of claims 1, 6, 11, and 21. The Applicants disagrees with this rejection, which paraphrases claim language in this application with references to Lien. Lien states than a hardened FPGA may be an embedded device in a larger integrated circuit. However, Lien does not describe how a core is embedded in a host integrated circuit, particularly when the core and the host integrated circuit have dissimilar pitches. Lien does not show or describe a program for automating routing for embedding a core.

Accordingly, Lien does not show or describe a "routing program" as claimed in claims 1, 6, 19, 25 and 27. Lien does not show or describe routing connections between an embedded core and an integrated circuit as claimed in claims 1, 6, 11 and 21. Lien does not show or describe "different"

pitches as claimed in claims 1, 6 and 21. Lien does not shown or describe either connection layers as claimed in claims 1 and 6 or an interconnect layer as claimed in claims 11 and 21.

It is respectfully submitted that claims 1, 6, 11 and 21 are all allowable in plain view of Lien. Furthermore, it is respectfully submitted that dependent claims 2-5, 7-10, 12-20 and 22-28 which depend upon allowable independent claims 1, 6, 11 and 21 are likewise allowable for at least the above-stated reasons.

It is respectfully submitted that the reference of Lien cited by the Examiner does not describe, show or suggest the claimed invention. Having addressed all issues set out in the Office Action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, Non-Fee Amendment, P.O. BOX 1450, Alexandria, VA 22313-1450, on December 24, 2003.

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